ML4012-28-4.5W

Technical Reference

QSFP28 Electrical Passive Loopback Module

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Table of Contents

1 General Description

The ML4012-28-4.5W is a QSFP28 passive electrical loopback module which is a hot pluggable form factor designed for high speed testing application for QSFP host ports. The ML4012-28-4.5W is designed for 100 Gigabit Ethernet applications and provides 4x28G RX and TX lanes, I2C module management interface and all the QSFP SFF hardware signals.
The ML4012-28-4.5W loops back 4-lane 28Gb/s transmit data from the host back to 4-lane 28Gb/s receive data port to the Host.

1.1 ML4012-28-4.5W QSFP 4x28G Passive Loopback Module | Key Features

- Operating up to 28G per Lane
- Supports 4x28G
- 4.5W max power dissipation
- QSFP MSA Form Factor
- Dual LED indicator
- Hot-Pluggable MSA footprint
- Temperature Range from 0°C to 70°C
- SFF-8436 Compliant EEPROM
- Low cost MSA Compliant loopback module

1.2 LED Indicator

The LED status is related to the ModSelL and LPMode signals status. The table below shows the LED status based on the signals status.

Signal Name	Signal Status	LED status
ModSelL	High	Green OFF
	Low	Green ON
LPMode	High	Amber OFF
	Low	Amber ON

1.3 Recommended Operating Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		0		70	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.5	V
Data Rate	Rb	Guaranteed to work at 28Gbps per Lane	0		28	Gbps
Input/output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0		4.5	W

2 Functional Description

2.1 Management Data Interface – I2C

The ML4012-28-4.5W supports the I2C interface. This QSFP28 specification is based on the SFF8436 specification. Address 128 Page00 is used to indicate the use of the QSFP28 memory map rather than the QSFP memory map.

2.2 I2C Signals, Addressing and Frame Structure

2.2.1 I2C Frame

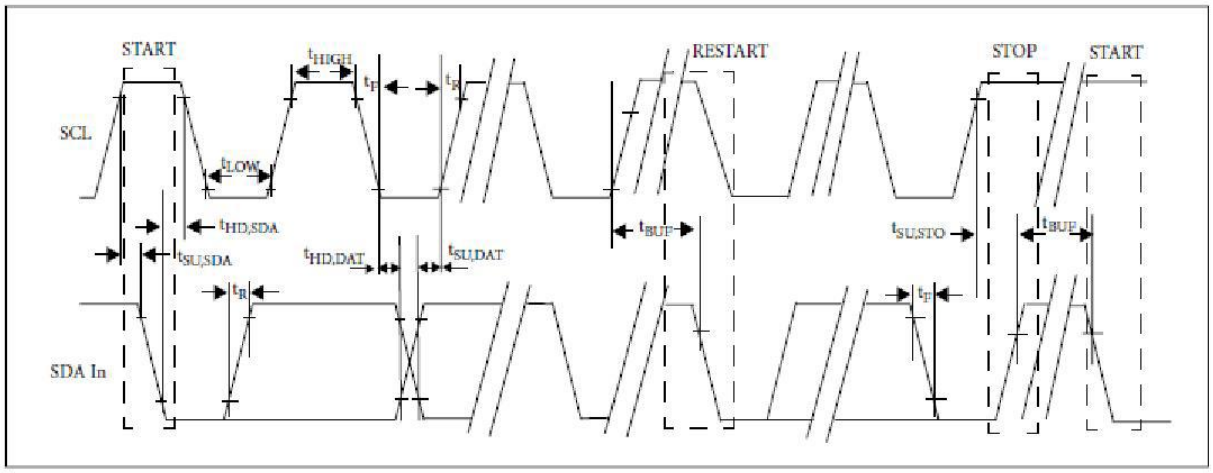

Figure 1: QSFP28 Timing Diagram

Before initiating a 2-wire serial bus communication, the host should provide setup time on the ModSelL line of all modules on the 2-wire bus. The host should not change the ModSelL line of

any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied. The 2-wire serial interface address of the QSFP28 module is 1010000X (A0h).

In order to allow access to multiple QSFP28 modules on the same 2-wire serial bus, the QSFP28 pinout includes a ModSelL or module select pin. This pin (which is pulled high or deselected in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module must not respond to or accept 2-wire serial bus instructions unless it is selected.

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}		400	kHz
Clock Pulse Width Low	t_{LOW}	1.3		us
Clock Pulse Width High	t_{High}	0.6		us
Time bus free before new transmission can start	t_{BUF}	1.3		us
Input Rise Time (400kHz)	$t_{R,400}$		300	ns
Input Fall Time (400kHz)	$t_{F,400}$		300	ns
Write Cycle Time	Twc		5	ms

2.2.2 Device Addressing and Operation

Serial Clock (SCL): The host supplied SCL input to QSFP transceivers is used to positive-edge clock data into each QSFP device and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven.

Master/Slave: QSFP transceivers operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Device Address: Each QSFP is hard wired at the device address A0h.
Multiple Devices per SCL/SDA: While QSFP transceivers are compatible with point-to-point SCL/SDA, they can share a single SCL/SDA bus by using the QSFP ModSelL line.

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the QSFP in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one-bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host shall be acknowledged by QSFP transceivers. Read data bytes transmitted by QSFP transceivers shall be acknowledged by the host for all but the final byte read, for which the host shall respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the QSFP management interface can be reset. Memory reset is intended only to reset the QSFP transceiver management interface (to correct a hung bus). No other transceiver functionality is implied.

1. Clock up to 9 cycles
2. Look for SDA high in each cycle while SCL is high
3. Create a Start condition as SDA is high

Device Addressing: QSFP devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 2. This is common to all QSFP devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 2: QSFP28 Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address (with ModSelL in the low state) the QSFP transceiver shall output a zero (ACK) on the SDA line to acknowledge the address.

2.3 I2C Read/Write Functionality

2.3.1 QSFP28 Memory Address Counter (Read AND Write Operations)

QSFP28 devices maintain an internal data word address counter containing the last address accessed during the latest read or write operation, incremented by one. The address counter is incremented whenever a data word is received or sent by the module. This address stays valid between operations as long as QSFP28 power is maintained. The address “roll over” during read and writes operations is from the last byte of the 128-byte memory page to the first byte of the same page.

2.3.2 Read Operations

2.3.2.1 Current Address Read

A current address read operation requires only the device address read word (10100001) be sent, see Figure 3 below.

		<-- QSFP+ ADDRESS --->																		
HOST	START	MSB						LSB	READ										NACK	STOP
		1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	x	1	
QSFP+										ACK	MSB							LSB		
											<---- DATA WORD ----->									

Figure 3: QSFP28 Current Address Read Operation

Once acknowledged by the QSFP+, the current address data word is serially clocked out. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

2.3.2.2 Random Read

A random read operation requires a “dummy” write operation to load in the target byte address as shown in Figure 4 below. This is accomplished by the following sequence.

		<- QSFP+ ADDRESS ->								<- MEMORY ADDRESS ->								
HOST	START	MSB						LSB	WRITE		MSB							LSB	
		1	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x	0
QSFP+										ACK									ACK

	<- QSFP+ ADDRESS ->																	
START	MSB						LSB	READ									NACK	STOP
	1	0	1	0	0	0	0	1	0	x	x	x	x	x	x	x	1	
									ACK	MSB						LSB		
										<---- DATA WORD n---->								

Figure 4: QSFP28 Random Read

The target 8-bit data word address is sent following the device address write word (10100000) and acknowledged by the QSFP+. The host then generates another START condition (aborting the dummy write without incrementing the counter) and a current address read by sending a device read address (10100001). The QSFP28 acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

2.3.2.3 Sequential Read

Sequential reads are initiated by a current address read (Figure 5). To specify a sequential read, the host responds with an acknowledgement (instead of a STOP) after each data word. As long as the QSFP28 receives an acknowledgement, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledgement.

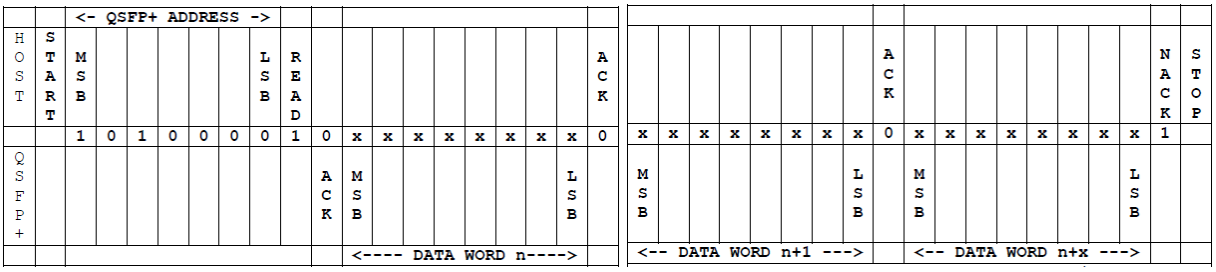

Figure 5: Sequential Address Read Starting at QSFP28 Current Address

2.4 Low Speed Signals

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

2.4.1 ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands and LED will be solid Green. The ModSelL allows the use of multiple QSFP28 modules on a single 2-wire interface bus. When the ModSelL is “High”, the module will not respond to or acknowledge any 2-wire interface communication from the host and the Green LED will be OFF. ModSelL signal input node is biased to the “High” state in the module. It is mandatory to force the ModSelL signal to Low in order to communicate with the module.

2.4.2 ResetL

The ResetL pin is pulled to Vcc in the QSFP28 module. A low level on the ResetL pin has no effect on the module operation.

2.4.3 LPMode

The LPMode is an input pin, it is pulled-up to VCC in the Module. When LPMode is Low, the module is in high power mode and the Amber LED is ON. When LPMode is high, the module is in low power mode and the Amber LED is OFF.

2.4.4 ModPrsL

ModPrsL is an output signal. It is grounded in the module. The ModPrsL is asserted “Low” when inserted and deasserted “High” when the module is physically absent from the host connector. For testing purpose ModPrsL can be controlled by the user as described in section 3.1.2.

2.4.5 IntL

IntL is an output pin, when “Low”, it indicates a possible module operational fault or a status critical to the host system. For testing purpose IntL can be controlled by the user as described in section 3.1.2.

2.5 QSFP Memory Map

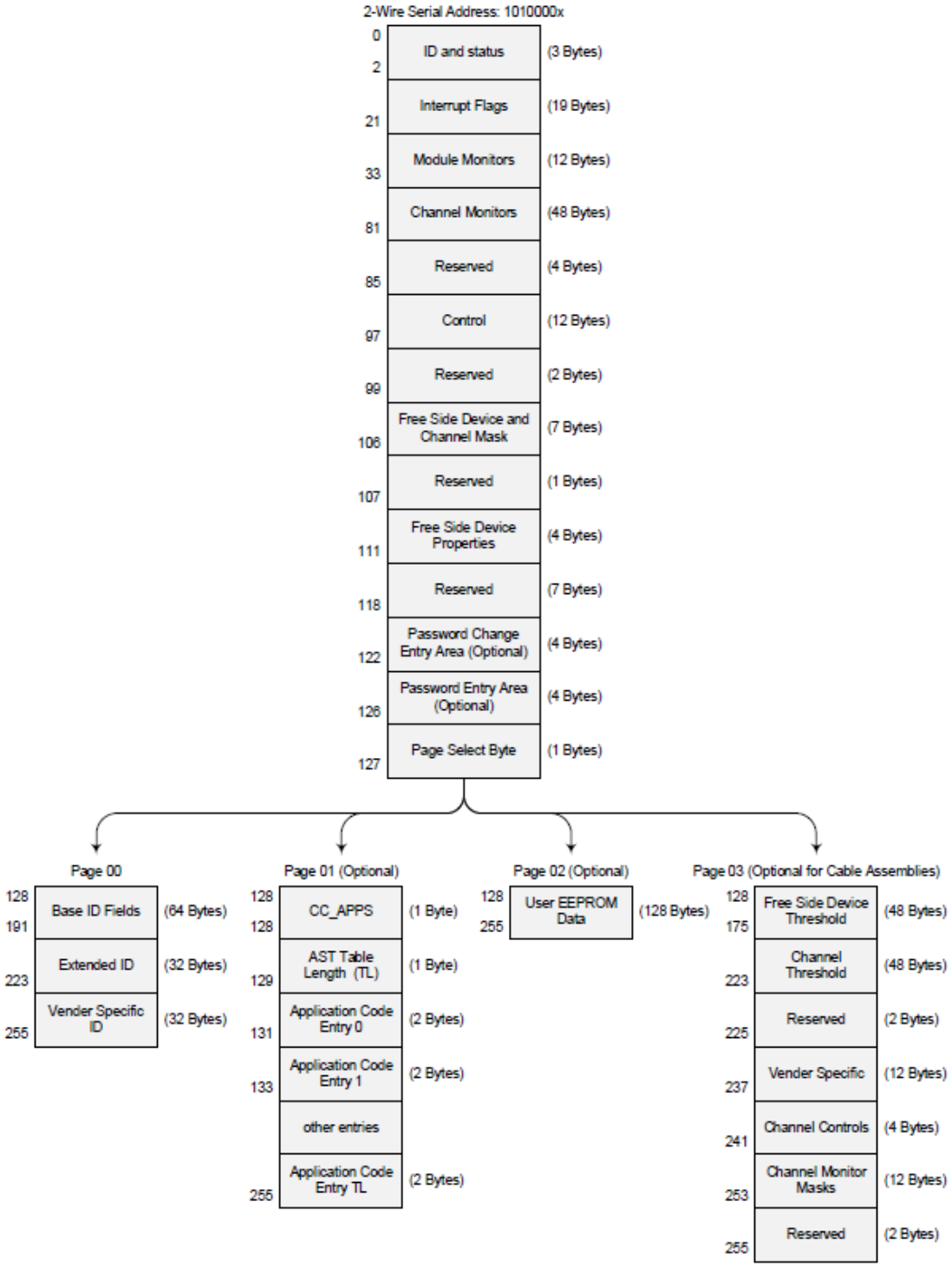

Figure 6: QSFP28 Memory Map

This section defines the Memory Map for QSFP transceiver. The interface is mandatory for all QSFP devices.

The structure of the memory is shown in Figure 6. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select

function. The structure also provides address expansion by adding additional upper pages as needed. For example, in Figure 6 upper pages 01 and 02 are optional. Upper page 01 allows implementation of Application Select Table, and upper page 02 provides user read/write space. The lower page and upper pages 00 and 03 are always implemented.

2.5.1 Lower Memory Map

The lower memory map is available for read/write functions. However, monitoring is not supported.

Byte Address	Description	Type
0	Identifier (1 Byte)	Read-Only
1-2	Status (2 Bytes)	Read-Only
3-21	Interrupt Flags (19 Bytes)	Read-Only
22-33	Module Monitors (12 Bytes)	Read-Only
34-81	Channel Monitors (48 Bytes)	Read-Only
82-85	Reserved (4 Bytes)	Read-Only
86-97	Control (12 Bytes)	Read/Write
98-99	Reserved (2 Bytes)	Read/Write
100-106	Module and Channel Masks (7 Bytes)	Read/Write
107-118	Reserved (12 Bytes)	Read/Write
119-122	Password Change Entry Area (optional) (4 Bytes)	Read/Write
123-126	Password Entry Area (optional) (4 Bytes)	Read/Write
127	Page Select Byte	Read/Write

3 Features Description

3.1 Control and Alarm Signals Configuration and Accessibility

The ML4012-28-4.5W module is terminated by a port expander chip. That allows to read and control the low speed signals over I2C bus. In order to allow any communication between the host and the module, it is mandatory to force the ModSelL signal to Low at first place.

The port expander has the device address 0x3A and includes configuration and control registers to communicate with. These registers have a default value upon power-up. So the user need to configure the register values each time after power-up, as described in the following sections.

3.1.1 Initialization and configuration

For proper module initialization and operation, two mandatory steps should be applied:

- Force ModSelL to Low
- Write 0xA0 to register 0x03 of device address 0x3A to configure I/O pins, as described in the table below

Device address	Register address	Set Value	Description	Type
0x3A	0x03	0xA0	Configure the port expander pins as input or output: Bit 7 = 1: configure LPMode pin as input Bit 5 = 1: Configure ResetL pin as input Bit 4 = 0: Configure INTL pin as output Bit 3 = 0: Configure ModPrsL pin as output Bit 2 = 0: Configure WP (write Protect) pin as output Bits 6, 1 and 0 = 0: not used	RW

3.1.2 Read and Control Signal Status

The Table below describes the control and alarm signals access to configure polarity, read input signals status and control output signals level.

Device address	Register address	Set Value	Description	Type
0x3A	0x02	-	The polarity inversion register allows polarity inversion of pins defined as inputs: 1b: polarity is inverted 0b: original polarity is retained	RW
	0x01	-	Control the output pins: -bit 4 (INTL) Write 1b : set INTL to High Write 0b : set INTL to Low -bit3 (ModPrsL) Write 1b: set ModPrsL to High Write 0b: Set ModPrsL to Low -bit 2 (Write Protect) Write 1b: set WP to High Write 0b: set WP to Low	RW
	0x00	-	Read the corresponding bit to check the input pin state: -Read bit 7 (LPMode): Read 1b: LPModeis High Read 0b: LPMode is Low -Read bit 5 (ResetL): Read 1b: ResetL is High Read 0b: ResetL is Low	RO

Details on low speed signals are described in the subsequent sections.

3.1.2.1 ModSelL

The ModSelL signal (module select) is an input signal that must be set to Low in order to allow the communication between the module and the host. The ModSelL signal affects the LED status, as described in the table below.

Signal Name	Signal Status	Communication status	LED Status
ModSelL	High	I2C Communication is stopped	Green LED OFF
	Low	I2C Communication is established	Green LED ON

3.1.2.2 LPMode

LPMode signal is an input signal that controls the power mode state and power consumption of the module. It also affects the LED status, as described in the table below. The user is allowed to read the LPModeL signal status from register 0x00 bit 7, as described in section 3.1.2.

Signal Name	Signal Status	Power Mode	LED Status
LPMode	High	Module is in Low Power Mode	Amber LED OFF
	Low	Module is in High Power Mode	Amber LED ON

3.1.2.3 Write Protect

The Write-Protect signal (WP) is intended to control the write operation on the EEPROM, it is pulled up to VCC in the module. The WP signal can be controlled from register 0x01 bit 2, as described in section 3.1.2.

Signal Name	Signal Status	Presence status
WP	Set to High	Write operation is inhibited
	Set to Low	Write operation is allowed

3.2 Temperature sensor

The ML4012-28-4.5W has an internal temperature sensor in order to continuously monitor the module temperature. The temperature sensor readings are accessible through I2C, at the device address 0x90. It is mandatory to force the ModSelL signal to Low at first place to establish I2C communication. Internally measured module temperature are represented in 8-bit signed two's complement format such that a reading of 0x00 corresponds to 0° C. The LSB unit

corresponds to 1 degree Celsius. The sensor covers the temperature range from -65°C (0xBF) to 130°C (0x7F).

The temperature data is reported in register 0x00 of device address 0x90. The sensor can be entered in standby mode, where the reported data is frozen, as described in the table below.

Device address	Register address	bit	Description	Type
0x90	0x00	7:0	Read reported temperature from register 0x00 LSB unit 1DegC	RO
	0x01	7	Configuration register write 0b: normal operation Write 1b: standby mode (data in register 0x00 is frozen)	RW

3.3 Power Dissipation

The ML4012-28-4.5W has a thermal spot allowing thermal emulation of the module. The power consumption follows the module power state. The max power dissipation of the module is 4.5W when it is in high power mode. When the module is entered in low power mode the power spot is turned off. The module power mode is controlled by LPMode signal, as described in section 3.1.2.2.

Control Signal	Signal Status	Module Power Mode	Power Consumption
LPMode	High	Low Power Mode	Power spot is OFF
	Low	High Power Mode	4.5W dissipation is ON

4 QSFP28 Pin Allocation

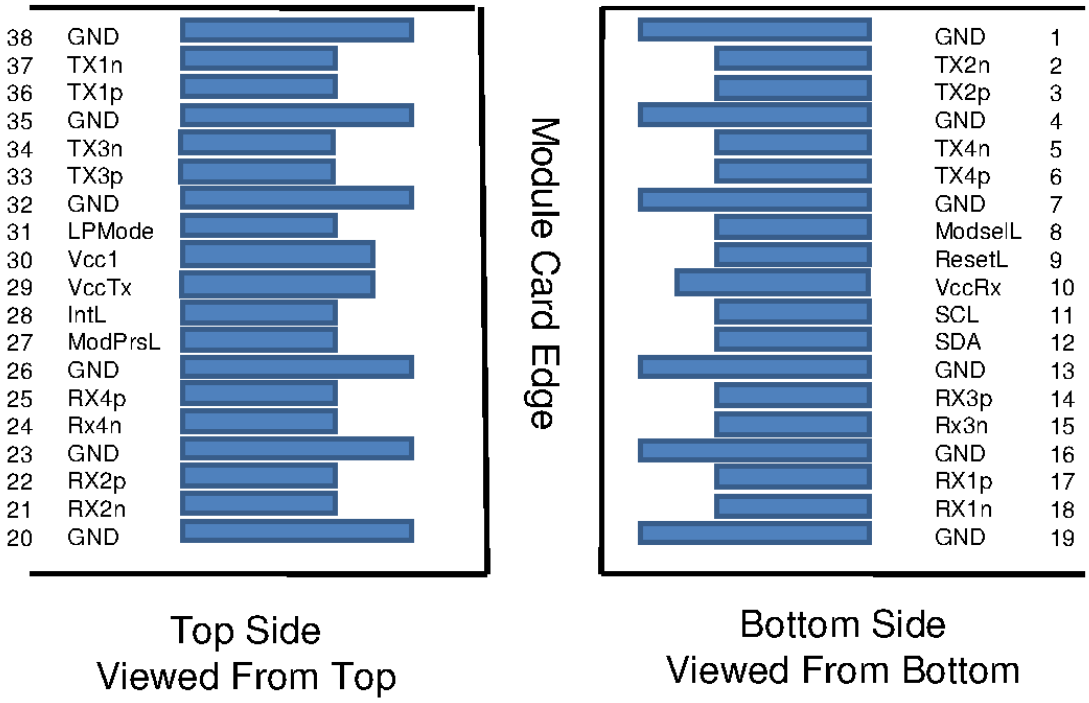

Figure 7: QSFP28 Pin Allocation

Pin#	Pin Name	Logic	Description
1	GND		Power Ground
2	Tx2n	CML-I	Transmitter Inverted Data Input
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input
4	GND		Power Ground
5	Tx4n	CML-I	Transmitter Inverted Data Input
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input
7	GND		Power Ground
8	ModSelL	LVTTL I	Module Select
9	ResetL	LVTTL I	Module Reset
10	Vcc Rx		+3.3 V Power supply receiver
11	SCL	LVCMOS – I/O	2-wire serial interface clock
12	SDA	LVCMOS – I/O	2-wire serial interface data
13	GND		Power Ground
14	Rx3p	CML-O	Receiver Non-Inverted Data Output
15	Rx3n	CML-O	Receiver Inverted Data Output
16	GND		Power Ground
17	Rx1p	CML-O	Receiver Non-Inverted Data Output
18	Rx1n	CML-O	Receiver Inverted Data Output
19	GND		Power Ground
20	GND		Power Ground
21	Rx2n	CML-O	Receiver Inverted Data Output

22	Rx2p	CML-O	Receiver Non-Inverted Data Output
23	GND		Power Ground
24	Rx4n	CML-O	Receiver Inverted Data Output
25	Rx4p	CML-O	Receiver Non-Inverted Data Output
26	GND		Power Ground
27	ModPrsl	LVTTL O	Module Present
28	IntL	LVTTL O	Interrupt
29	Vcc Tx		+3.3 V Power supply transmitter
30	Vcc1		+3.3 V Power Supply
31	LPMode	LVTTL I	Low Power Mode
32	GND		Power Ground
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input
34	Tx3n	CML-I	Transmitter Inverted Data Input
35	GND		Power Ground
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input

5 High Speed Signals

High speed signals are electrically looped back from TX side to RX side of the module, all differential TX pairs are connected to the corresponding RX pairs, and the signals are AC coupled as specified in the QSFP28 HW specifications.
The Passive traces connecting TX to RX pairs are designed to support a data rate up to 28Gbps.

Revision History

Revision number	Date	Description
0.1	2/25/2022	▪ Preliminary